REMARKS

Claims 2-13, 16-19, and 21 are pending in the application with the present amendments. Claims 1, 14-15 and 20 are cancelled. The undersigned reaffirms the election, without traverse, of the Group I claims 1-20 that was made by telephone on March 10, 2004. Accordingly, the sole Group II claim 21 stands withdrawn herein as being directed to a non-elected invention. The present amendment responds to the Examiner's rejection of claims 7-9 under 35 U.S.C. §112 by amending claim 7 to now recite "initial *column* address bits", such term having antecedent basis in claim 6 from which claim 7 depends.

In the Office Action, claims 6-7 and 15 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,959,911 to Krause et al. ("*Krause*"). Claims 1-20 were also rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,260,127 B1 to Olarig et al. ("*Olarig*"). For the reasons set forth below, Applicants submit that the presently pending claims overcome the rejections made by the Examiner. Reconsideration and withdrawal of the rejections is respectfully requested.

As amended herein, the invention recited in claim 2 provides a method for accessing a memory array of a chip (IC) through a set of row address bits and a set of translated column address bits. The translated column address bits are translated from initial column address bits output by a memory manager of the chip. The initial column address bits are arranged to identify a column memory location which is defined according to a first format. By contrast, the translated column address bits identify a column memory location defined according to a second format. Thus, as recited in claim 2, a memory manager of an integrated circuit outputs an address for accessing memory locations defined according to a first format, and, as made possible by the

invention, can access locations of a memory of the chip that are defined according to a second format. In addition, as recited in claim 2, while the row address bits and the initial column address bits are received at different times, the row address bits and the translated column address bits are presented simultaneously to access a desired row and column memory location in the memory.

By contrast, neither *Krause* nor *Olarig* teaches or suggests the features recited in amended claim 2. Neither *Krause* nor *Olarig* teaches or suggests accessing a desired memory location of a chip by a memory manager of that same chip, wherein at least some of the initial column address bits output by the memory manager are translated prior to presenting them as translated column address bits, together with the row address bits, to access the desired row and column memory location. Both *Krause* and *Olarig* merely show systems in which addresses are converted for accessing memories that are located on different chips. *Olarig*, col. 7, lns. 31 *et seq*. Nor do *Krause* or *Olarig* teach or suggest presenting the row address bits and a set of translated column address bits *simultaneously* to access the desired memory location, when the row address bits identify a row memory location and the translated column address bits identify a column memory location. Rather, the row address and the column address are presented at different times. For example, as taught by *Olarig*, the row address is presented when the memory controller asserts "row address strobe" (RAS) and the column address is presented when the memory controller asserts "column address strobe" (RAS). *Krause*, col. 6, lns. 29-31, *Olarig*, col. 8, lns. 27-33. Accordingly, claim 2 is allowable over *Krause* and *Olarig*.

Similar recitations to those of claim 2 are now found in independent claims 6, 10 and 16 as amended herein, making these claims allowable now, as well. As all others of the presently elected claims depend from either claims 2, 6, 10 or 16, they are allowable

over *Krause* and *Olarig*. Accordingly, the rejections must be withdrawn.

Support for the present amendments herein is provided *inter alia*, at page 1, lns. 13-14, page 6, lns. 1-7, page 7, lns. 4-17.

Based on the foregoing, it is believed that all of the rejections in the Office Action have been overcome. Accordingly, reconsideration and allowance is respectfully requested. No fee is due with the present amendment, there being no increase in the number of pending claims or independent claims above that which has already been paid for.

Respectfully submitted,

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